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10/626,242	07/24/2003	James A. Zollo	7463-10	9999

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EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 03/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,242	ZOLLO ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *February 11, 2005 and interview summary.*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-20 and 22-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-20 and 22-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *July 24, 2003*.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *0305*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election with traverse of group II, claims 15-20 and 22-24, in the reply filed on February 11, 2005 is acknowledged. Regarding specie election, the applicant elected specie reading on figure 6D, claims 15-20 and 22-24 (see interview summary).

The traversal is on the ground(s) that, "the existing claim language in its broadest form appears to encompass all the alternatives recited by the examiner. In this regards the method in claim 1 recites applying an adhesive / bonding layer between substrate cores and applying conductive layers. There are no limitations in the broadest method claim as to methods of performing these steps since "applying" should not be restricted in interpretation to just plating or sputtering or bonding or gluing. Thus, the apparatus would not necessarily be made using materially different processes in this regard to make the product in view of the broadest claim".

This is not found persuasive because: (a) The limitation "patterning at least one among the top conductive layer", in claim 1, line 11, is a specific step of forming a pattern out of the conductive layer on the substrate, which can be performed by different processes, as stated in the restriction requirement. Therefore, it is clear that the product could be made by different process. (b) Further, it is not the individual claim, which is restricted. The restriction is between two distinct groups of the invention. One group is directed to a method of forming a multilayer circuit board and the other group is directed to a multilayer circuit board structure. Therefore, claim 1 is not individually restricted but is a part of the group. The reasons for restriction as stated in the previous actions are for the restriction of groups and not for individual claims.

The requirement is still deemed proper and is therefore made FINAL.

Non-elected claims, claims 1-14 and 21, are cancelled by the applicant. Claims 15-20 and 22-24 are examined for patentability.

Drawings

2. The drawings are objected to because the figures are improperly cross hatched. All of the parts shown in section, and only those parts, must be cross-hatched. The cross-hatching patterns should be selected from those shown on page 600-114/115 of the MPEP based on the material of the part. See also 37 CFR 1.84(h)(3) and MPEP § 608.02.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 15-19 are objected to because of the following informalities: Regarding claim 15, the claim is directed to a structure of a multilayer circuit board with the related structural limitations. It appears that the phrase "the steps of", line 1, is inadvertently added into the claim language and may be removed from the claim. For the examination purpose the phrase is not considered a as part a of the claim language. Claims 16-19 depend upon claim 15 and inherit the same deficiency. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 15, 16, 20 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Carpenter et al., US Patent No. 5,495,665.

Regarding claim 15, Carpenter et al., in figure 8, discloses a multilayer circuit board having inverted microvias, comprising at least a first substrate core (1) and a

second substrate core (2) each of said first substrate core and said second substrate core having a top conductive layer (5 and 6 respectively) on at least a top side; a microvia (not identified in figure 8 but shown in detail as element 8, in figure 2) on a bottom side of at least one among the first substrate core (1) and the second substrate core (2, alternately), wherein the microvia would reach to the top conductive layer (5) on at least the top side of at least one among the first substrate core (1) and the second substrate core (2); a conductive layer (not identified in figure 8 but shown in detail as element 9 in figure 3-5) applied to the microvia interconnecting a bottom conductive layer (10) to the top conductive layer of at least one among the first substrate core and the second substrate core; an adhesive/bonding layer (14) between at least the first substrate core (1) and the second substrate core (2); a hole (15', as labeled in figure 6) through the first substrate core, the adhesive/bonding layer and the second substrate core; a conductive layer (as shown in figure 7 and 8, column 5, line 53-57) applied to the hole to interconnect at least two among the top conductive layer (5) of the first substrate core (1), the top conductive layer (6) of the second substrate core (2), the bottom conductive layer of the first substrate core, and the bottom conductive layer of the second substrate core.

Regarding claim 16, Carpenter et al., further discloses the top conductive layer (5) of the first substrate core (1) and the top conductive layer (6) of the second substrate core, comprises a predefined pattern, (see figure 8, column 6, line 1-3.

Regarding claim 20, Carpenter et al., in figure 8, discloses a multilayer circuit board, comprising: a plurality of substrate cores (1, 2); an adhesive/bonding layer (14) between at least two among the plurality of substrate cores; a microvia (not identified in figure 8 but shown in detail as element 8, in figure 2) in each of at least two of the plurality of substrate cores, wherein the microvia includes a conductive interconnection (not identified in figure 8 but shown in detail as element 9 in figure 3-5) between a top conductive surface (5, 6 respectively) and a bottom conductive surface (10,11 respectively) of each of the at least two of the plurality of substrate cores (1 and 2), wherein at least a microvia in a first substrate core (1) is arranged to be inverted (see figure 8) relative to a microvia in a second substrate core (2) and a plated through-hole (through hole as seen in figure 8, but not labeled) through the plurality of substrate cores (1 and 2) and the adhesive/bonding layer (14), wherein the plated through-hole connects at least two among the top conductive (5 and 6) surfaces and the bottom conductive surfaces of the plurality of substrate cores.

Regarding claim 24, Carpenter et al., in figure 8, discloses a multilayer circuit board, comprising: a plurality of substrate cores (1 and 2); an adhesive/bonding layer (14) between at least two among the plurality of substrate cores; a microvia (8, as labeled in figure 2) in at least one among the plurality of substrate cores (1 and 2), wherein the microvia includes a conductive interconnection (9, as labeled in figure 3-5) between a top conductive surface (5) and a bottom conductive surface (10) of at least one among the plurality of substrate cores, and a plated through-hole (through hole as

seen in figure 8, but not labeled) through the plurality of substrate cores and the adhesive/bonding layer, wherein the plated through-hole connects at least two (5,6) among the top conductive surfaces and the bottom conductive surfaces of the plurality of substrate cores.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 17-19, 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al., US Patent No. 5,495,665, applied to claims 15 and 20 above, in view of Kim et al., US Patent No. 6,580,036.

Regarding claim 17, the applicant is further claiming an external dielectric layer on at least one among the topside of the first substrate core (1) and the topside of the second substrate core (2) and an external conductive layer on the external dielectric layer.

Carpenter et al., discloses all the features of the claimed invention including first substrate core and the second substrate core, as applied to claim 15 above, however fails to disclose an external dielectric layer on at least one among the top side of the first

substrate core and the top side of the second substrate core and an external conductive layer on the external dielectric layer.

Kim et al., in figure 5, discloses a multilayer printed circuit board with external dielectric layers (21a) on top of first substrate core (21b) with an external conductive layer (22c) on topside of the external dielectric layer (21a).

As evinced from Kim et al., it is well known in the art to provide external dielectric layers with respective external conductive layer. The additional layer with respective conductive layer will increase the trace density and resultant component mounting density of the circuit board structure. Further, additional layer will facilitate better routing of the traces.

A person of ordinary skill in the art at time of applicant's invention would have recognized the advantage of providing an external dielectric layer to increase the component mounting density of the circuit board structure and to facilitate better routing of the traces on / in the board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter et al., with an external dielectric layer on the top side of the first substrate core and an external conductive layer on the external dielectric layer, as taught by Kim et al., in order to increase the component mounting density of the circuit board structure and to facilitate better routing of the traces on / in the board.

Regarding claim 18, the modified structure of Carpenter et al., (in combination of Kim et al.), discloses all the features of the claimed invention including the external dielectric layer, as applied to claim 17 above, however, fails to disclose the hole further goes through the external dielectric layer and the external conductive layer. The through hole of Carpenter et al., as shown in figure 8, goes though the first substrate core, the adhesive/bonding layer and the second substrate core.

Kim et al., in figure 5, further discloses a through hole (42), which goes through the external dielectric layer (22a) and external conductive layer (22c), to have electrical connection to external conductive layers.

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to further modify the structure of Carpenter et al. in order to extend the hole through the external dielectric layer and external conductive layer for providing electrical connection to external layers. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to further modify the circuit board of Carpenter et al., extending the hole through the external dielectric layer, as further taught by Kim et al., in order to have connection to external layers.

Regarding claim 19, the modified structure of Carpenter et al., further discloses the conductive layer applied to the hole interconnects at least two among the top conductive layer (5, Carpenter et al., figure 8), of the first substrate core (1, Carpenter et al., figure 8), the top conductive layer (6, Carpenter et al., in figure 8) of the second substrate core (2, Carpenter et al., in figure 8), the bottom conductive layer of the first

substrate core, the bottom conductive layer of the second substrate core, and the external conductive layers.

Regarding claim 22, the applicant is further claiming an external dielectric layer on at least one among the topside of the first substrate core and the topside of a last substrate core and an external conductive layer on the external dielectric layer.

Carpenter et al., discloses all the features of the claimed invention including first substrate core (1) and a last (second) substrate core (2), as applied to claim 20 above, however fails to disclose an external dielectric layer on at least one among the top side of the first substrate core (1) and the top side of the last substrate core (2) and an external conductive layer on the external dielectric layer.

Kim et al., in figure 5, discloses a multilayer printed circuit board with external dielectric layers (21a) on top of first substrate core (21b) with an external conductive layer (22c) on topside of the external dielectric layer (21a).

As evinced from Kim et al., it is well known in the art to provide external dielectric layers with respective external conductive layer. The additional dielectric layer with respective external conductive layer will increase the trace density and resultant component mounting density of the circuit board structure. Further, additional layer will facilitate better routing of the traces.

A person of ordinary skill in the art at time of applicant's invention would have recognized the advantage of providing an external dielectric layer to increase the

component mounting density of the circuit board structure and to facilitate better routing of the traces on / in the board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Carpenter et al., with an external dielectric layer on the top side of the first substrate core and an external conductive layer on the external dielectric layer, as taught by Kim et al., in order to increase the component mounting density of the circuit board structure and to facilitate better routing of the traces on / in the board.

Regarding claim 23, the modified structure of Carpenter et al., (in combination of Kim et al.), discloses all the features of the claimed invent including the external dielectric layer, as applied to claim 22 above and a through hole (through hole of Carpenter et al., as shown in figure 8) through the plurality of substrate cores (1 and 2) and adhesive bonding layer (14). Carpenter et al., further discloses the through hole connecting at least two layers, top conductive layers (5 and 6) of first and second substrate cores, however, fails to disclose a plated through-hole extending through the external dielectric layer.

Kim et al., in figure 5, further discloses a through hole (42), which goes through the external dielectric layer (22a) and external conductive layer (22c), to have electrical connection to external conductive layers.

It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to further modify the structure of Carpenter et al. in order to extend

the hole into the external dielectric layer for providing connection to external layers. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to further modify the circuit board of Carpenter et al., extending the plated through hole through the external dielectric layer, as further taught by Kim et al., in order to have connection to external layers.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arai et al., US Patent No. 5,315,072, in figure 1(B), discloses a printed wiring board having inverted blind via.

Frankeny et al. US Patent No. 5,509,200, in figure 12, discloses a circuit board structure with inverted vias.

Chong et al., US Patent No. 5,758,413, in figure 9, discloses a circuit board structure with vertically stacked blind via.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IBPatel

Ishwar (I. B.) Patel
Examiner
Art Unit: 2841
March 2, 2005